IN THE SPECIFICATION:

Please replace the paragraph on page 5, lines 11-12 with the following paragraph:

-- Figure 3B illustrates a logic gate level netlist model and a Verilog netlist representing model digital circuit illustrated in Figure ~~2~~ 3A. --

Please replace the paragraph on page 6, lines 14-19 with the following paragraph:

-- Data is transferred along network 16 to and from each of the other components in computer system 14. Data representing a physical circuit to be tested is input by I/O devices 22 to memory 20. A program for generating a netlist model for the circuit is input to memory 20 from storage medium ~~16~~ 21. CPU 18 runs the program and outputs the netlist model to I/O devices 22, so that the netlist may be used in ATPG. The program for generating the netlist model is described below in greater detail. --

Please replace the paragraph on page 7, lines 9-16 with the following paragraph:

-- Figure 3B illustrates a logic gate level netlist model 27 and a Verilog netlist 28 representing model digital circuit 1' illustrated in Figure ~~2~~ 3A. Netlist model 2 of digital circuit 1 from Figure 1 is incorporated into netlist model 27. Netlist model 27 also includes virtual delay elements 24 and 26, which are described as flip-flops that latch the values at inputs in_{24} and in_{26} to outputs out_{24} and out_{26} when vclk1 and vclk2 are high. In Verilog netlist 28, vclk1 and vclk2 are designated as a type of wire and implicitly used as control points for an ATPG tool. This is equivalent to declaring them as and using them as primary inputs. --